DEC 15 2004

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To:	Examiner Baumeister	**From:**	Peter Medley
Fax:	703-872-9306	**Date:**	December 15, 2004
Phone:	571-272-1722	**Pages:**	21
Re:	09/658,732 36856.919	**CC:**	

•Comments:

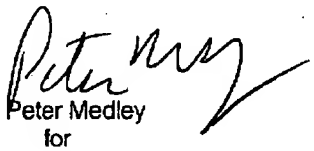
Examiner Baumeister,

Please find attached hereto the following documents for the above-identified application:

1) Appeal Brief; and

2) Credit Card Form PTO-2038.

Respectfully submitted,



Peter Medley
for
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(Registration Number 56,125)

DEC 15 2004

CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that this correspondence is being transmitted to Group Art Unit 2815, 703-872-9306, addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date: December 15, 2004

Peter M. Medley

PATENT
36856.919

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Makoto INAI et al. Serial No.: 09/658,732 Filed: September 11, 2000 Title: FIELD-EFFECT SEMICONDUCTOR DEVICE	Art Unit: 2815 Examiner: B. Baumeister

APPEAL BRIEF UNDER 35 U.S.C. § 134(a)

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is an Appeal pursuant to 35 U.S.C. § 134(a) from the Examiner's rejection of claims 1-10 and 12-15 in the outstanding Office Action dated May 18, 2004.

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REAL PARTY IN INTEREST:

The real party of interest is the assignee, Murata Manufacturing Co., Ltd., 10-1 Higashikotari 1-chome, Nagaokakyo-shi, Kyoto-fu 617-8555 JAPAN.

RELATED APPEALS AND INTERFERENCES:

Applicants, assignee, and the undersigned attorney of record are not aware of any other appeals or interference involving this application.

STATUS OF CLAIMS:

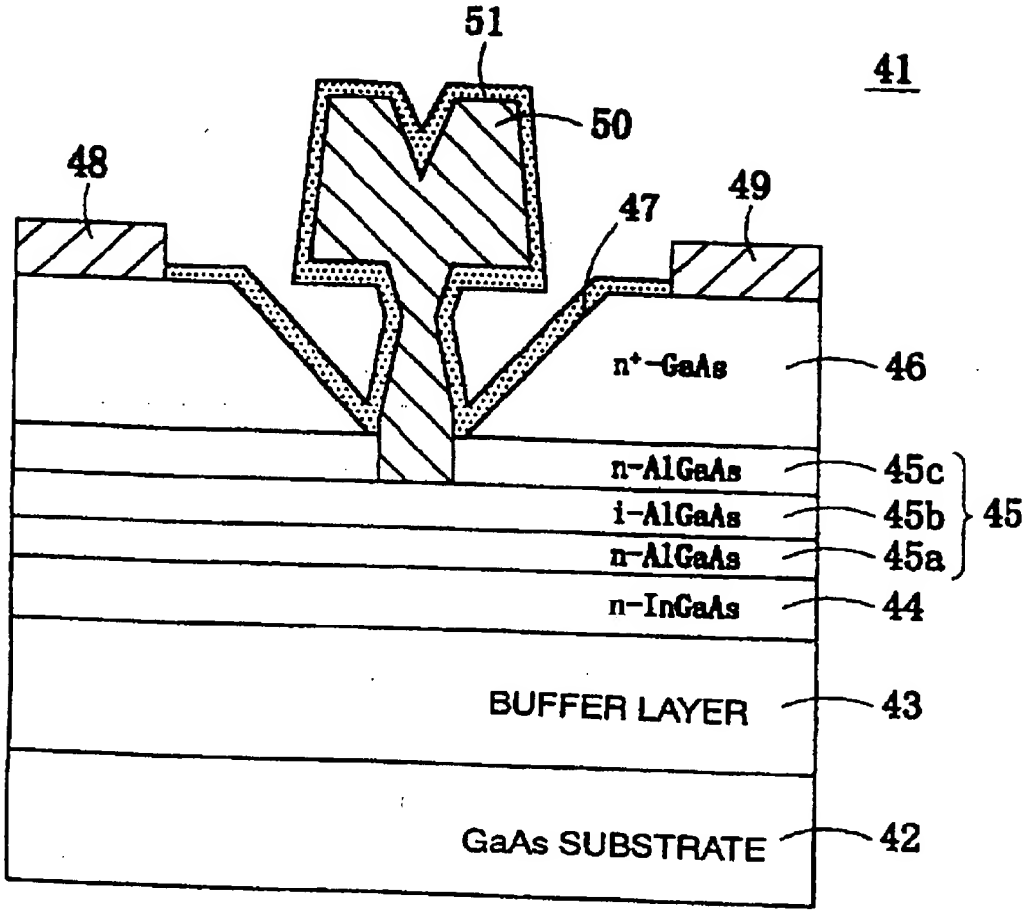
Claim 11 has been cancelled.

Claims 1-10 and 12-15 have been at least twice rejected and are the subject of this appeal.

STATUS OF AMENDMENTS:

Applicants have not submitted any amendment after the outstanding Office Action, dated May 18, 2004.

SUMMARY OF CLAIMED SUBJECT MATTER:



Claim 1

The field-effect semiconductor device of claim is generally depicted in **Fig. 4**. **Fig. 4** is depicted above, where the n- prefix means n-doped, the n+- prefix means heavily n-doped, and the i- prefix means undoped.

The channel layer is generally depicted as reference symbol **44** in **Fig. 4**.

The contact layer is generally depicted as reference symbol **46** in **Fig. 4**.

The semiconductor structure formed between the channel layer and the contact layer is generally depicted as reference symbol **45**, including reference symbols **45a**,

45b, and **45c**, in **Fig. 4**. In the "First Embodiment" section, starting the on page 10 of the originally filed Specification, the semiconductor structure is described by the term "barrier layer."

That the semiconductor structure has an electron-affinity different from those of the channel layer and the contact layer is discussed, for example, in the paragraph bridging pages 11 and 12 of the originally filed Specification.

The ohmic electrode formed on the contact layer is generally depicted as reference symbol **49** in **Fig. 4**.

The Schottky electrode formed on the semiconductor structure is generally depicted as reference symbol **50** in **Fig. 4**.

That both of the first junction face and the second junction face are iso-type heterojunctions is discussed, for example, in the paragraph bridging pages 11 and 12 of the originally filed Specification.

That the semiconductor structure is composed of a single material and includes at least two semiconductor layers is discussed, for example, in the paragraph bridging pages 11 and 12 of the originally filed Specification.

Claim 15

The field-effect semiconductor device of claim 15 is generally depicted in **Fig. 4**.

The channel layer is generally depicted as reference symbol **44** in **Fig. 4**.

The contact layer is generally depicted as reference symbol **46** in **Fig. 4**.

The semiconductor structure formed between the channel layer and the contact layer is generally depicted as reference symbol **45**, including reference symbols **45a**, **45b**, and **45c**, in **Fig. 4**.

That the semiconductor structure includes at least two semiconductor layers is discussed, for example, in the paragraph bridging pages 11 and 12 of the originally filed Specification.

That the semiconductor structure has an electron-affinity different from those of the channel layer and the contact layer is discussed, for example, in the paragraph bridging pages 11 and 12 of the originally filed Specification.

The ohmic electrode formed on the contact layer is generally depicted as reference symbol **49** in **Fig. 4**.

The Schottky electrode formed on the semiconductor structure is generally depicted as reference symbol **50** in **Fig. 4**.

That the junction between the layers of the semiconductor device is an iso-type heterojunction is generally discussed, for example, in the paragraph bridging pages 8 and 9 and in the second full paragraph on pages 11 and 12 of the originally filed Specification.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL:

The Examiner's rejection of claims 1-10 and 12-15 under 35 U.S.C. §103(a) as being unpatentable over Sawada et al. ("A Super Low-Noise AlGaAs/InGaAs/GaAs DC-HFET with 0.15 μm Gate-Length") in view of Enoki et al. ("Delay Time Analysis for 0.4- to 5- μm -Gate InAlAs-InGaAs HEMT's").

ARGUMENT:

Claims 1-10 and 12-15 are improperly rejected under 35 U.S.C. §103(a) as being unpatentable over Sawada et al. in view of Enoki et al.

The Examiner rejected claims 1-10 and 12-15 under 35 U.S.C. §103(a) as being unpatentable over Sawada et al. in view of Enoki et al.

Applicants agree with the Examiner that Sawada et al. does not anticipate the claims. The Examiner has relied upon Enoki et al. to allegedly cure various deficiencies in Sawada et al.

In paragraph c. on page 3 of the outstanding Office Action, the Examiner alleged:

> It would have been obvious to one of ordinary skill in the art at the time of the invention to have modified the Sawada [et al.] n-AlGaAs barrier layer by providing an additional undoped layer between the top and bottom portions (or restated, by temporarily stopping and restarting the dopant supply during the growth of the barrier layer) for the purpose of enhancing the Schottky barrier of the gate while simultaneously providing a source/drain series resistance that is reduced relative to if the upper portion of the barrier was undoped as taught by Enoki [et al.]; and also for the purpose of providing both of these advantages while simultaneously obviating the need for the additional masking steps that would be required to achieve the structure of Sawada [et al.]'s FIG. 6 embodiment wherein the dopant implant is provided for only the [source/drain] region.

First, in the first paragraph under section "II. Device Structure and Performance" of Enoki et al., Enoki et al. state, "The upper n+-InAlAs layer is designed to reduce the source and drain series resistance." That is, Enoki et al. teach that the highly doped n+-InAlAs layer, not, as alleged by the Examiner, the undoped i-InAlAs layer, is used to reduce the source and drain series resistance. Thus, providing an additional undoped layer in the barrier layer of Fig. 1 of Sawada et al. would not reduce the source and the drain series resistance. In fact, as discussed below and admitted to by the Examiner in the last paragraph on page 7 of the outstanding Office Action, the addition of the undoped layer to the device in Fig. 1 of Sawada et al. would increase the resistance.

Second, Applicants do not understand the Examiner's reference to Fig. 6 of Sawada et al. as it is directed to a different embodiment that clearly has a much

different structure than the embodiment shown in Fig. 1 of Sawada et al., which the Examiner has relied upon to allegedly teach various features of the Applicants' claims 1 and 15. This is clearly shown by the section title under which Fig. 6 of Sawada et al. is discussed: "New Device Structure." Fig. 6 of Sawada et al. clearly fails to teach or suggest, at least, a contact layer.

Third, in the first paragraph under the section "II. Device Structure and Performance" of Enoki et al., Enoki et al. state, "The undoped InAlAs layer between two highly doped InAlAs layers is to enhance the Schottky barrier of the gate metal" (emphasis added). However, the Examiner has failed to provide any evidence that one of ordinary skill in the art at the time of Applicants' invention would have expected the effect of enhancing the Schottky barrier could be achieved by providing an undoped AlGaAs layer in between two doped AlGaAs layers. Enoki et al. fails to teach or suggest that the effect of enhancing the Schottky barrier produced by providing an undoped InAlAs layer between two highly doped InAlAs layers would be produced if an undoped AlGaAs layer were provided between two doped AlGaAs layers. In fact, Enoki et al. fails to teach or suggest anything at all about AlGaAs layers.

Fourth, in paragraph a. on page 5 of the outstanding Office Action the Examiner explained, "... the more heavily n-doped a barrier layer is ... the lower the gate Schottky barrier is." Thus, by the Examiner's reasoning, the device in Fig. 1 of Sawada et al. would have a higher Schottky barrier than the device in Fig. 1 of Enoki et al. because the barrier layer of the device in Fig. 1 of Sawada et al. has less than half of the n-doping of the barrier layer of the device in Fig. 1 of Enoki et al. The Examiner has failed to explain why one of ordinary skill in the art at the time of Applicants' invention would have desired to further enhance the Schottky barrier of the barrier layer of the device in Fig. 1 of Sawada et al.

Fifth, in the paragraph bridging pages 6 and 7 of the outstanding Office Action, the Examiner alleged that Enoki et al. teaches "including an undoped layer between sandwiching heavily doped barrier layers and in contact with the gate metal will increase the gate Schottky barrier relative to if the undoped layer was not present, at least when (1) the undoped layer is composed of the same base composition as the doped barrier

layers (i.e., the doped/undoped/doped barrier layers form two homojunctions); and (2) the doped barrier layers are n-doped on the order of 10^18 (i.e., at least a few orders of magnitude greater than the undoped layer) ... ."

However, contrary to the Examiner's allegation, Enoki et al. does not teach this. In the first paragraph under the section "II. Device Structure and Performance," Enoki et al. state, "The doping density for n+-InAlAs was 4 X 10^{18} cm^{-3}. The undoped InAlAs layer between two highly doped InAlAs layers is to enhance the Schottky barrier of the gate metal." That is, Enoki et al. teaches that an undoped InAlAs layer between two highly n-doped InAlAs layers having a doping density of 4 X 10^{18} cm^{-3} enhances the Schottky barrier of the gate metal. The Examiner has failed to explain how this very specific teaching of Enoki et al. substantiates his much broader allegations.

In the next sentence in the paragraph bridging pages 6 and 7 of the outstanding Office Action, the Examiner alleges, "The 'allegation' that this effect also applies to semiconductor material systems other than InAlAs is based on the well-understood physics principles that in an undoped III-V semiconductor, the Fermi energy level is positioned approximately midway between the conduction and valence band, and that n-doping III-V semiconductor materials shifts the Fermi energy level towards the conduction band." However, the Examiner has failed to provide any evidence to substantiate this allegation.

Sixth, the Examiner alleged, in the last paragraph on page 7 of the outstanding Office Action:

> Enoki [et al.] also teaches that the further inclusion of the upper highly n-doped barrier layer—that forms a junction with the superposed highly n-doped, lower bandgap InGaAs contact layer—reduces the series resistance, at least sufficiently to allow the HFET to operate as intended. As such, the further inclusion of an undoped layer composed of the same material as the rest of Sawada's barrier layer would not cause the barrier to possess unsatisfactorily high resistance because the additional presence of the upper, highly n-doped region of the AlGaAs barrier layer that forms a junction with the GaAs [source/drain] contact layers in

> Sawada [et al.] would sufficiently reduce the [source/drain] series resistance to allow the Sawada [et al.] HFET to operate as intended, as taught by Enoki [et al].

The Examiner has failed to provide any evidence to support this allegation. Even if the Examiner's allegation that the effect of the junction between the n-doped AlGaAs barrier layer and the n-doped GaAs contact layer is to lower the resistance is true, that effect would be present before modifying the device of Fig. 1 of Sawada et al. to have an undoped layer. That is, the effect of adding an undoped layer to the device of Fig. 1 of Sawada et al. is to increase the resistance. Further, the Examiner has failed to provide any evidence that one of ordinary skill in the art would have considered the modified device of Fig.1 of Sawada et al. having a higher resistance to be satisfactory. In fact, Sawada et al. clearly teaches, as acknowledged by the Examiner, that it is desirous to have a reduced resistance in the discussion of the "new device structure" in Fig. 6.

Accordingly, Applicants respectfully request that the Examiner's rejection of claims 1-10 and 12-15 under 35 U.S.C. § 103(a) as being unpatentable over Sawada et al. in view of Enoki et al. be reversed.

Claims 1-10 and 12-15 are allowable over Sawada et al. and Enoki et al.

Accordingly, Applicants respectfully submit that the rejection of claims 1-10 and 12-15 under 35 U.S.C. § 103(a) as being unpatentable over Sawada et al. and Enoki et al. should be reversed and that claims 1-10 and 12-15 are allowable.

Respectfully submitted,

Date: December 15, 2004

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CLAIMS APPENDIX:

Claim 1 (previously presented): A field-effect semiconductor device comprising:

a channel layer;

a contact layer;

a semiconductor structure having an electron-affinity different from those of the channel layer and the contact layer and formed between the channel layer and the contact layer, the semiconductor structure having a first junction face between the semiconductor structure and the channel layer and having a second junction face between the semiconductor structure and the contact layer;

an ohmic electrode formed on the contact layer; and

a Schottky electrode formed on the semiconductor structure;

wherein both of the first junction face and the second junction face are iso-type heterojunctions; and

the semiconductor structure is composed of a single material and includes at least two semiconductor layers.

Claim 2 (previously presented): A field-effect semiconductor device according to claim 13, wherein the channel layer and the doped layer of the semiconductor structure at the first junction face are each n-type doped layers, and the contact layer and the doped layer of the semiconductor structure at the second junction face are each n-type doped layers.

Claim 3 (previously presented): A field-effect semiconductor device according to claim 2, wherein the channel layer and the semiconductor structure at the first junction face each have a dopant concentration of 1×10^{18} cm^{-3}, and the contact layer and the semiconductor structure at the second junction face each have a dopant concentration of 1×10^{18} cm^{-3}.

Claim 4 (previously presented): A field-effect semiconductor device according to claims 1 or 2, wherein the electron-affinity of the semiconductor structure is smaller than those of the channel layer and the contact layer.

Claim 5 (previously presented): A field-effect semiconductor device according to claim 3, wherein the electron-affinity of the semiconductor structure is smaller than those of the channel layer and the contact layer.

Claim 6 (original): A field-effect semiconductor device according to claim 4, wherein the semiconductor structure is composed of AlGaAs.

Claim 7 (original): A field-effect semiconductor device according to claim 5, wherein the semiconductor structure is composed of AlGaAs.

Claim 8 (original): A field-effect semiconductor device according to claims 1, 2 or 3, wherein the channel layer is composed of InGaAs.

Claim 9 (previously presented): A field-effect semiconductor device according to claim 8, wherein the electron-affinity of the semiconductor structure is smaller than those of the channel layer and the contact layer.

Claim 10 (original): A field-effect semiconductor device according to claim 8, wherein the semiconductor structure is composed of AlGaAs.

Claim 11 (canceled).

Claim 12 (previously presented): A field-effect semiconductor device according to claim 14, wherein the channel layer and the doped layer of the semiconductor structure at the first junction face are each n-type doped layers, and the contact layer

and the doped layer of the semiconductor structure at the second junction face are each n-type doped layers.

Claim 13 (previously presented): A field-effect semiconductor device according to claim 1, wherein the first junction face between the channel layer and the semiconductor structure and the second junction face between the contact layer and the semiconductor structure are iso-type heterojunctions; the channel layer and the semiconductor structure at the first junction face are each formed of doped layers; the contact layer and the semiconductor structure at the second junction face are each formed of doped layers; and the semiconductor structure includes an undoped layer intermediate the doped layers thereof.

Claim 14 (previously presented): A field-effect semiconductor device according to claim 13, wherein the Schottky electrode is in contact with the undoped layer.

Claim 15 (previously presented): A field-effect semiconductor device comprising:

a channel layer;

a contact layer;

a semiconductor structure having an electron-affinity different from those of the channel layer and the contact layer, the semiconductor structure having at least two layers;

an ohmic electrode formed on the contact layer; and

a Schottky electrode formed on the semiconductor structure; wherein

the semiconductor structure is formed between the channel layer and the contact layer, and where a junction between said layers of the semiconductor device is a heterojunction, the junction is an iso-type heterojunction.

EVIDENCE APPENDIX:

None.

RELATED PROCEEDINGS APPENDIX:

None.